In the Claims

Claims 1-12. (Canceled).

Claim 13 (Original): A method of reconfiguring a data cache for caching data in a computing device, the data cache operating at a plurality of levels in a memory hierarchy and comprising a portion having a variable size operating at a first level of the plurality of levels, the method comprising:

(a) storing performance information for the data cache;

(b) determining, from the performance information, whether the data cache has a miss rate exceeding a threshold;

(c) determining whether the variable size is equal to a maximum size; and

(d) if the miss rate exceeds the threshold and the variable size is not equal to the maximum size, controlling the data cache to increase the variable size.

Claim 14 (Original): The method of claim 13, further comprising:

(e) if the miss rate does not exceed the threshold or the variable size is equal to the maximum size, (i) determining, from the performance information, an optimal data cache configuration which optimizes a number of cycles per instruction in the computing device and (ii) setting the data cache to the optimal data cache configuration.

Claim 15 (Original): The method of claim 14, wherein, in each of a plurality of time periods during which the data cache operates, steps (a)-(c) and one of steps (d) and (e) are performed.

Claim 16. (Original): The method of claim 15, wherein each of the time periods is a fixed number of cycles of the computing device.

Claim 17. (Original): The method of claim 15, wherein each of the time periods is a time period in which the computing device performs a subroutine.

Claim 18. (Original): The method of claim 15, wherein:

the data cache is designated as either stable or unstable; and

steps (a)-(c) are performed only during intervals in which the data cache is designated as unstable.

Claim 19. (Original) The method of claim 18, further comprising, during intervals in which the data cache is designated as stable:

(f) determining, from the performance information, whether the data cache is actually unstable; and

(g) if the data cache is actually unstable, (i) designating the data cache as unstable and (ii) setting the variable size to a minimum value.

Claim 20. (Original) The method of claim 19, wherein:

the performance indication comprises a hit counter for a second portion of the data cache which is outside the portion having the variable size; and

when the data cache is designated as stable and the hit counter is below a hit counter threshold, the second portion of the data cache is bypassed.

Claim 21. (Original) The method of claim 13, wherein:

the data cache comprises tag arrays and data arrays;

the first level is L1; and

in the portion having the variable size, the tag arrays and the data arrays are read in series.

Claim 22. (Original): A method of reconfiguring a translation look-aside buffer for use in a computing device, the translation look-aside buffer having a variable size, the method comprising:

(a) storing performance information for the translation look-aside buffer;

(b) determining, from the performance information, whether the translation look-aside buffer has a miss rate exceeding a first threshold;

(c) determining, from the performance information, whether the translation look-aside buffer has a usage less than a second threshold;

(d) if the miss rate exceeds the first threshold, controlling the translation look-aside buffer to increase the variable size; and

(e) if the use is less than the second threshold, controlling the translation look-aside buffer to decrease the variable size.

Claim 23. (Original): The method of claim 22, wherein, in each of a plurality of time periods during which the data cache operates, steps (a)-(c) and one of steps (d) and (e) are performed.

Claim 24. (Original): The method of claim 23, wherein each of the time periods is a fixed number of cycles of the computing device.